Solutions for RISC-V

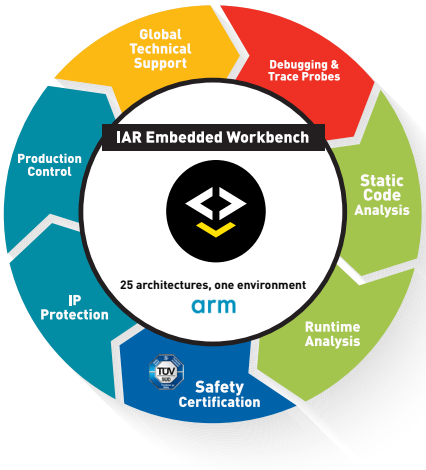
Enabling powerful embedded applications based on 32- and 64-bit RISC-V devices

As the leading commercial solutions vendor for RISC-V, IAR provides stable and future-proof technology as well as global technical support.

IAR Embedded Workbench for RISC-V is a complete toolchain with excellent optimization technology to ensure developers that the application fits the required needs and optimizes the utilization of on-board memory and necessary speed. For safety-critical development, a functional safety edition of the toolchain is available. For efficient CI/CD workflows, IAR Build Tools for RISC-V are available enabling automated builds on Ubuntu, Red Hat or Windows.

Key capabilities

- Renowned compiler technology
- Outstanding performance through sophisticated optimization technology
- Extensive debugging capabilities through the state-of-the-art debugger C-SPY
- Support for the RV32I, RV32E and RV64I base instruction sets
- Support for the instruction extensions such as M, A, F, D, C, P, B, N, CMO, Zfinx together with the Andes DSP, Performance and CoDense extensions.
- Integration with our feature-rich debugging probe I-jet and I-jet Trace
- Customized extensions support
- Stack protection
- Easy-to-use example projects to get up and running on hardware quickly



Future-proof solutions in a fast-moving market

The RISC-V International organization is moving fast with optional additions to the instruction set, debug and trace infrastructure and other aspects of the architecture. We have been part of this organization since 2018, participating in selected working groups and committed to support standardized functionality relevant for embedded systems.

We are continuously adding support for new devices and extensions as well as new features in our development solutions for RISC-V.

Integrated static analysis

The static analysis tool IAR C-STAT is integrated in IAR Embedded Workbench and helps to find potential issues in the code by doing an analysis on the source code level. IAR C-STAT is covering the SEI CERT C Coding Standard, which provide rules for developing safe, reliable and secure systems in the C programming language. IAR C-STAT also checks compliance with rules as defined by coding standards including MISRA C:2004, MISRA C++:2008 and MISRA C:2012, as well as hundreds of rules based on CWE (the Common Weakness Enumeration).

Customized extensions

The standardized ability to extend the base instruction set with your own customized extensions is a prominent feature of the RISC-V instruction set. This ability can be used in innovative ways to tailor your own SoC design to specific workloads, to for example balance energy, speed and code size requirements. IAR Embedded Workbench for RISC-V lets you add support for such customized extensions in an easy and intuitive way.

Functional safety and security

Our RISC-V tools are available in functional safety editions, certified by TÜV SÜD according to the requirements of IEC 61508, ISO 26262, IEC 62304, EN 50128, EN 50657, IEC 60730, ISO 13849, IEC 62061, IEC 61511 and ISO 25119. The standardization of security features is an ongoing work in RISC-V International and we are committed to supporting features relevant for embedded systems.

Automated workflows with cross-platform benefit

The IAR Build Tools for Arm are streamlined for automated build and test processes supporting modern and scalable build server topologies on Ubuntu, Red Hat and Windows for CI/CD pipelines including Virtual Machines, Containers (Docker) and Self-hosted Runners.

Advanced debugging and trace capabilities

By making use of the advanced debugging tools, you can optimize the working time of your team when investigating issues and testing your application. The IAR I-jet debug probe facilitates advanced visualization of the application behavior. In addition, the IAR I-jet Trace probe enables powerful code coverage and profiling data capabilities in IAR Embedded Workbench and traces every single executed instruction in an application.